What is claimed is:

1. An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

2. The circuit of claim 1, wherein the driving signal control circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

3. The circuit of claim 1, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response

to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

4. The circuit of claim 1, wherein the comparing circuit includes:

a comparator connected between a first node and a ground voltage and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated.

5. The circuit of claim 1, wherein the comparing circuit includes:

a comparator connected between a first node and a second node and comparing the reference voltage to the internal voltage to generate the driving signal;

a first switching circuit connected between the external power voltage and the first node and cutting off the external power voltage applied to the comparator when the control signal is activated; and

a second switching circuit connected between the second node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated.

6. The circuit of claim 1, wherein the comparing circuit includes:

a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal; and

a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated.

7. The circuit of claim 1, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

8. The circuit of claim 1, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

9. The circuit of claim 1, wherein the control signal generating circuit activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.

10. An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a comparing circuit for comparing a reference voltage to an internal voltage to generate a comparing signal;

a switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

11. The circuit of claim 10, wherein the driving signal control circuit includes an NMOS transistor which has a drain connected to a driving signal generating terminal for generating the driving signal, a gate to which the control signal is applied, and a source connected to a ground voltage.

12. The circuit of claim 10, wherein the internal voltage driving circuit includes a PMOS transistor which has a source to which the external power voltage is applied, a gate to which the driving signal is applied, and a drain connected to an internal voltage generating terminal for generating the internal voltage, wherein the PMOS transistor turns the internal voltage to a reference voltage level in response to the driving signal and turns the internal voltage to an external power voltage level when the driving signal is inactivated.

13. The circuit of claim 10, wherein the switching circuit includes a CMOS transmission gate which transmits the comparing signal as the driving signal when the control signal is inactivated.

14. The circuit of claim 10, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

15. The circuit of claim 10, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

16. The circuit of claim 10, wherein the control signal generating circuit activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.

17. An internal voltage generating circuit of a semiconductor device, comprising:

a control signal generating circuit for generating a control signal according to a number of data bits;

a first internal voltage generating circuit for receiving a reference voltage and an internal voltage to turn the internal voltage to a reference voltage level;

a second internal voltage generating circuit for receiving an external power voltage to turn the internal voltage to an external power voltage level;

a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and

a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

18. The circuit of claim 17, wherein the first switching circuit includes a CMOS transmission gate which supplies the external power voltage to the first internal voltage generating circuit when the control signal is inactivated.

19. The circuit of claim 17, whereint the switching circuit includes a CMOS transmission gate which supplies the external power voltage to the second internal voltage generating circuit when the control signal is inactivated.

20. The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

21. The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

22. The circuit of claim 17, wherein the control signal generating circuit activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.

23. An intern voltage generating circuit of a semiconductor device, comprising:

a first internal voltage generating circuit for comparing a first reference voltage to a first internal voltage and turning the first internal voltage to a first reference voltage level;

a second internal voltage generating circuit for comparing a second reference voltage to a second internal voltage to turn the second internal voltage to a second reference voltage level or to turn the second internal voltage to an external power voltage level in response to a control signal; and

a control signal generating circuit for generating the control signal according to a number of data bits.

24. The circuit of claim 23, wherein the second internal voltage generating circuit includes:

a comparing circuit for comparing the second reference voltage to the second internal voltage to output a driving signal when the control signal is inactivated and for being disabled when the control signal is activated;

an internal voltage driving circuit for receiving the external power voltage and outputting the second internal voltage in response to the driving signal; and

a driving signal control circuit for inactivating the driving signal when the control signal is activated and for being disabled when the control signal is inactivated.

25. The circuit of claim 23, wherein the second internal voltage generating circuit includes:

a comparing circuit for comparing the second reference voltage to the seocnd internal voltage to generate a comparing signal;

a switching circuit for transmitting the comparing signal as a driving signal when the control signal is inactivated;

a driving signal control circuit for inactivating the driving signal when the control signal is activated; and

an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal.

26. The circuit of claim 23, wherein the second internal voltage generating circuit:

a first internal voltage generating circuit for receiving the second reference voltage and the second internal voltage to turn the second internal voltage to a second reference voltage level;

a second internal voltage generating circuit for receiving an external power voltage to turn the second internal voltage to an external power voltage level;

a first switching circuit for supplying the external power voltage to the first internal voltage generating circuit when the control signal is inactivated; and

a second switching circuit for supplying the external power voltage to the second internal voltage generating circuit when the control signal is activated.

27. The circuit of claim 23, wherein the control signal generating circuit activates or inactivates the control signal using a fuse option.

28. The circuit of claim 23, wherein the control signal generating circuit activates or inactivates the control signal using a bonding option.

29. The circuit of claim 23, wherein the control signal generating circuit activates or inactivates the control signal by receiving a mode setting signal together with a mode setting command.